REMARKS

The present application was filed on July 15, 2003 with claims 1-19. Claims 1 and 3-19 remain pending and stand rejected. Claims 1, 18 and 19 are the pending independent claims.

Claims 1, 3, 4 and 6-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Boggio et al., "NetworkDesigner - Artifex - OptSim: A Suite of Integrated Software Tools for Synthesis and Analysis of High Speed Networks," Optical Networks Magazine, Sept/Oct 2001, pages 27-41 (hereinafter "Boggio") in view of Sun et al., "Simulation Studies of Multiplexing and Demultiplexing Performance in ATM Switch Fabrics," Performance Engineering in Telecommunications Network Teletraffic Symposium, 14-16 Apr. 1993, pages 21/1 – 21/5 (hereinafter "Sun").

Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Boggio in view of Sun in further view of Ishida et al., "A 10-GHz 8-b Multiplexer/Demultiplexer Chip Set for the SONET STS-192 System," IEEE Journal of Solid-State Circuits, Vol. 26, No. 12, Dec. 1991, pages 1936-1943 (hereinafter "Ishida").

In this response, Applicants respectfully traverse the rejections under §103(a) and respectfully request reconsideration of the present application in view of the remarks below.

Claim 1 recites a method of simulating the operation of at least one switch fabric comprising a plurality of integrated circuits using a software-based development tool. This method includes the steps of providing in the software-based development tool an interface permitting user control of one or more configurable parameters of the switch fabric, and automatically generating, without requiring further user input, a simulation configuration for the switch fabric based on current values of the configurable parameters, the simulation configuration specifying interconnections between the integrated circuits which satisfy the current values of the configurable parameters. As discussed in the specification at, for example, page 1, line 16, to page 2, line 19; page 3, lines 15-18; and page 5, lines 21-28, this method advantageously allows for automated determination of an appropriate configuration of integrated circuits within a simulation of a switch fabric, thus reducing the time required for such simulation.

The combined teachings of Boggio and Sun not only fail to teach or suggest at least the limitations of providing a user interface permitting user control of one or more configurable parameters of a switch fabric, and automatically generating a simulation configuration for the

switch fabric specifying interconnections between the integrated circuits of the switch fabric, but both Boggio and Sun actively teach away from such limitations by instead disclosing arrangements which assume a single fixed switch fabric configuration. See Boggio at page 30, column 1, first paragraph ("In every network design, either manually or automatically generated, all network elements are modeled as having a fixed 'back-plane' with specific connectors.") (emphasis added) and Sun at page 21/3, sixth paragraph ("In this tool only fixed routing mechanism is [sic] implemented. A routing table is used to specify the next queues taken by the cells to their destinations.") (emphasis added). Thus, Boggio and Sun only disclose conventional techniques for simulation of a fixed configuration which fail to achieve the advantages of the present invention in automated determination of an appropriate configuration of integrated circuits within a simulation of a switch fabric.

Applicants further submit that Sun and Boggio are not analogous prior art and therefore cannot form the basis for a rejection under 35 U.S.C. §103. Even if the Examiner's assertion, found in paragraph 14 of the Office Action, that Sun and Boggio "are both directed to the modeling of and simulation of a network," were true, it would still be insufficient to establish them as analogous prior art; see, e.g., Wang Lab. v. Toshiba Corp., 993 F.2d 858, 864 (Fed. Cir. 1993) (holding that "art is not in the same field of endeavor as the claimed subject matter merely because it relates to memories.").

Whereas the limitations of claim 1 are directed to generation of an optimal device-level simulation configuration for at least one switch fabric, Boggio is directed toward network-level simulations rather than device-level simulations of such individual network components as switch fabrics. See, e.g., Boggio at page 28, column 1, last paragraph ("This paper specifically focuses on the benefits of combining together three tools to form an integrated suite for the virtual prototyping of optical networks: NetworkDesigner, Artifex, and OptSim.").

Additionally, the Sun reference actively teaches away from the limitations directed to the simulation of at least one switch fabric (e.g., providing an interface permitting user control of one or more configurable parameters of the switch fabric) by indicating at page 21/3, first paragraph, that "[d]imensioning the switch fabric" beyond the "simple configuration" involving a single switch fabric is "beyond the scope" of its disclosure.

With regard to motivation to combine Sun with Boggio, the Examiner provides the following statement in the Office Action at paragraph 15:

> It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the software development tool for an optical network as disclosed in Boggio et al to include the modeling of a multistage switch fabric . . . . as taught in Sun et al since Sun et al teaches a method for modeling a switch fabric with basic components for simulation to study multiplexing and demultiplexing performance in a network, enabling the switch fabric to be modeled without losing generality.

Applicants respectfully submit that the proffered statement fails to provide sufficient objective motivation for the combination. The Federal Circuit has stated that when patentability turns on the question of obviousness, the obviousness determination "must be based on objective evidence of record" and that "this precedent has been reinforced in myriad decisions, and cannot be dispensed with." In re Sang-Su Lee, 277 F.3d 1338, 1343 (Fed. Cir. 2002). Moreover, the Federal Circuit has stated that "conclusory statements" by an Examiner fail to adequately address the factual question of motivation, which is material to patentability and cannot be resolved "on subjective belief and unknown authority." Id. at 1343-1344. The statement listed above is believed to be a conclusory statement based on the type of "subjective belief and unknown authority" that the Federal Circuit has indicated provides insufficient support for an obviousness rejection. More specifically, the statement above is using the benefit obtained from a combination as a motivation for that combination and thus constitutes impermissible hindsight. Additionally, the statement is suggesting that would be obvious to modify a software development tool for an optical network to include the modeling of a multistage switch fabric where, as discussed above, these are distinct and non-analogous fields of endeavor.

It is thus believed that the collective teachings of Boggio and Sun fail to meet the limitations of claim 1. Independent claims 18 and 19 contain limitations similar to those of claim 1 are believed to be patentable for similar reasons.

Dependent claims 3-17 are believed allowable for at least the reasons identified above with regard to claim 1. Additionally, at least one of these claims defines separately patentable subject matter.

For example, dependent claim 5 recites the method of claim 1 in which the integrated circuits comprise integrated circuits of a designated chip set utilizable in the switch fabric. In characterizing the Ishida reference as allegedly meeting this additional limitation, the Examiner relies primarily on page 1936, column 1 of Ishida, which the Examiner contends "teaches an

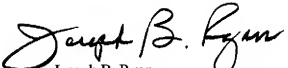
ultra high speed 8-b multiplexer and demultiplexer chip set that has been developed for the synchronous optical network (SONET) as a key component of next-generation optical fiber communication systems that will require higher data bit rates for future increases in transmission capacity." (paragraph 24)

However, within the optical networking context to which Ishida (unlike the present invention) is limited, multiplexers and demultiplexers are distinct components from a switch fabric. See, e.g., Harry G. Perros, Connection-Oriented Networks: SONET/SDH, ATM, MPLS, and Optical Networks 198 (2005) ("An [optical switch] consists of amplifiers, multiplexers/demultiplexers, a switch fabric, and a CPU."); George N. Rouskas & Lisong Xu, Optical Packet Switching, in Emerging Optical Network Technologies: Architectures, Protocols and Performance 111, 113 (Krishna M. Sivalingam & Suresh Subramaniam, eds.) (2005) ("[A] generic [optical packet switching] node . . . . consists of a set of multiplexers and demultiplexers, an input interface, a space switch fabric with associated optical buffers (i.e. fiber delay lines) and wavelength converters, an output interface, and a switch control unit.").

Accordingly, Ishida fails to teach or suggest the additional limitation of dependent claim 5 wherein the integrated circuits comprise integrated circuits of a designated chip set utilizable in the switch fabric. Instead, it merely teaches integrated circuits of a designated chip set utilizable in a multiplexer and demultiplexer. Thus, the Ishida reference fails to supplement the above-noted fundamental deficiencies of Boggio and Sun relative to claim 5.

In view of the foregoing, claims 1 and 3-19 are believed to be in condition for allowance.

Respectfully submitted,



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